HMIC Improvements

Timothy Boles, James Brogle, David Hoag, Margaret Barter, Joseph Bukowski
September, 2019
Problem Statement – Historical HMIC

New Concepts
• Vertically Etched <1-1-1> Crystal Axis Substrates
• Phosphorous Substrates
• Discrete PIN Diodes
• Monolithic PIN Switches

Preliminary Discrete PIN Diodes/Switch Results

Monolithic High Power PIN Diode Switches & Limiters

Multi ”I” Region PIN Diodes

Future Actions/Summary
Heterolithic Microwave Integrated Circuit

- Development Initiated - 1991
- Two Different Materials Bonded Into ONE Structure
- Wafer Scale Technology - Joining Glass & Silicon

Enables Monolithic Circuit Solutions That Reduce Both Size & Cost

- SURMOUNT PIN/Schottky, PIN Diode Switches, Schottky Diode Mixers, VVA’s, Limiters
- High Q Capacitors & Inductors
- True 3-D RF and Mechanical Structures

Glass Die With Islands Of Embedded Silicon

- Fundamental Circuit Design
- Low Loss Conductive Ground Plane
- Minimum Parasitic Capacitances

Fundamental Technology In Place – mid1990s

Product Improvements Via Layout - Power Handling & Frequency Response
Historical HMIC

➢ <1-0-0> - N+ (<0.0045 Ω-cm) Substrates

➢ Wet Trench Etch
  • Only Controlled Etch Available for Deep Trenches
  • ODE (KOH) – Preferentially Etch 1-1-1 planes (54.7 Degree angle)
  • Pattern Distortion After Etch
    • Circles => Octagons
    • Rectangles => Require “Mickey Mouse” Ears

➢ <1-1-1> Substrates – Crystal Planes Etched Uniformly

➢ ICP/HRM Bosch Process
  • Vertical Etch
  • Shape/Crystal Structure/Doping Independent
HMIC Improvements - <1-1-1> Arsenic

> <1-0-0> - N+ (<0.0045 Ω-cm) – 900µm Thick Substrates – Present State

> Unique HMIC Issue
  • Wafer Bow After Glass Bonding
  • Impacts Process Time/Cost
  • Requires Overnight Slow Cool Annealing of Glass
  • Multiple Slow Cool Cycles – Function of Circuit Design/Layout
  • Occasional Wafer Breakage

> ICP/HRM Bosch Process
  • Enables Etching of <1-1-1> Substrates

> <1-1-1> Heavily Doped Cz Substrates
  • Modeling Predicts Reduced Wafer Bow
  • Higher Electron Mobility on <1-1-1> Material – Lower Series Resistance (Rs)
  • More Dangling Bonds at <1-1-1> Surface - Higher Surface Leakage
HMIC Improvements - <1-1-1> Phosphorus

- <1-0-0> - N+ (<0.0045 Ω-cm) – Present State

- ICP/HRM Bosch Process
  - Enables Etching of <1-1-1> Substrates

- <1-1-1> - Cz - N+ Cz Phosphorous Doped Substrates
  - 0.001 Ω-cm
  - 5x Reduction in Cathode Resistance
  - Higher Q/Lower Rs Diode
  - Use Existing HMIC Designs – Surmount PINs/Schottkys, Switches, Limiters, VVAs, Mixers

- Expected Differences
  - Lower Rs
    - Higher Electron Mobility on <1-1-1> Material
    - Reduced Cathode Resistance
  - Series Diodes - Lower Insertion Loss
  - Shunt Diodes – Higher Isolation
  - More Dangling Bonds at <1-1-1> Surface - Higher Surface Leakage
Test Vehicles
Initial Results

- Low Barrier Discrete Schottky Diode
  SURMOUNT – HSSVL02

- Discrete PIN Diode SURMOUNT
  PV3025

- Three Substrate Variants
  - <1-0-0> 0.0045 \( \Omega \)-cm Arsenic (Control)
  - <1-1-1> 0.006 \( \Omega \)-cm Arsenic
  - <1-1-1> 0.0017 \( \Omega \)-cm Phosphorus

- <1-1-1> - N+ (<0.006 \( \Omega \)-cm) – Arsenic Substrates
  - No Difference in Bow/Flatness
  - Expected Improvement

- <1-1-1> - N+ (<0.0017 \( \Omega \)-cm) Phosphorous Substrates
  - Electrical Improvement Produced Mixed Results
Results
SURMOUNT Schottky Diode – HSSVL02

> DC Results

> All Variants

> $V_b$ for the Control Group was a Bit High – Behaving Like a Medium Barrier Diode

> $V_b$ for both the <1-1-1> As and <1-1-1> P Substrates Approx Lower Spec Limit for Low Barrier Schottky Diodes

> $I_r$ for both the <1-1-1> As and <1-1-1> P Wafers was Higher than the Control but still well within Spec Limit

> $V_f$ and $C_{j0}$ for all variants within Spec Limit

> $R_d$ (Slope Resistance) 33% Lower for the <1-1-1> P Wafers
Results
SURMOUNT Schottky Diode – HSSVL02

- RF Testing
- Plot of Series Resistance @ 500 MHz
- Essentially Identical $R_s$ Performance - <1-0-0> As (Control Std) and <1-1-1> As
- Combined with DC results - <1-0-0> As & <1-1-1> As can be used Interchangeably

- <1-1-1> Phosphorus Substrates Resulted in 40% Lower $R_s$ Compared to <1-0-0> As Control
- <1-1-1> Phosphorus Substrates – Higher Sensitivity/Lower Insertion Loss
Results
SURMOUNT Schottky Diode – HSSVL02

> RF Testing

> Plot of Series Resistance vs Frequency @20 mA Bias Current

> <1-0-0> 0.0045 Ω-cm As (Control Std) had the Highest RF $R_s$ – Almost 9 ohms

> The <1-1-1> 0.006 Ω-cm As Substrate Variant had a $R_s$ that was 13% lower at approx. 8 ohms

> <1-1-1> 0.0017 Ω-cm Phosphorus Substrates Resulted in a 50% Lower High Frequency $R_s$ Compared to <1-0-0> As Control essentially validating the DC Slope Resistance Results

> <1-1-1> Phosphorus Substrates lower $R_s$ => Higher Sensitivity/Lower Insertion Loss
Results
SURMOUNT PIN Diode – PV3025

DC Results

- $I_r$ for all Variants well within Spec Limit
- $I_r$ for <1-1-1> P Wafers had the Lowest Reverse Leakage

<table>
<thead>
<tr>
<th>PV3025 SURMOUNT PIN Diode</th>
<th>$I_r$</th>
<th>$V_f$</th>
<th>$C_{j0}$</th>
<th>DC Slope Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PV3025 Spec Limit</td>
<td>1000nA Max</td>
<td>700mV - 1200mV</td>
<td>0.01pF-0.56pF</td>
<td>&lt;3.5 ohms</td>
</tr>
<tr>
<td>(&lt;1-0-0&gt;) 0.0045 As Substrates</td>
<td>17.2</td>
<td>797.3</td>
<td>0.495</td>
<td>2.7</td>
</tr>
<tr>
<td>(&lt;1-1-1&gt;) 0.006 As Substrates</td>
<td>30.7</td>
<td>795.7</td>
<td>0.481</td>
<td>2.7</td>
</tr>
<tr>
<td>(&lt;1-1-1&gt;) 0.0017 P Substrates</td>
<td>9.5</td>
<td>795.5</td>
<td>0.484</td>
<td>2.6</td>
</tr>
</tbody>
</table>

- $V_f$, $C_{j0}$, and $R_d$ (Slope Resistance) for All Variants Essentially Identical and Well Within Spec Limits
Results
SURMOUNT PIN Diode – PV3025

> RF Testing

> Plot of Series Resistance @ 500 MHz

> Essentially Identical $R_s$ Performance - <1-0-0> As (Control Std) and <1-1-1> Phosphorus Substrates

> <1-1-1> Phosphorus Substrates and the <1-0-0> As Control Resulted in approx. 10% Lower $R_s$ Compared to <1-1-1> As Variant

> <1-1-1> Phosphorus Substrates and the <1-0-0> As Control – Lower Insertion Loss/Higher Isolation
Results
SURMOUNT PIN Diode – PV3025

- RF Testing
- Plot of Series Resistance versus Frequency @ 20 mA of Bias Current
- RF $R_s$ Performance of the Much Different than DC Slope Resistance, $R_d$
- <1-1-1> Phosphorus Substrates Ranged from 8% to 18% Lower $R_s$ Compared to either the <1-0-0> As Control or the <1-1-1> As Variant

- Predictive that the <1-1-1> Phosphorus Substrates should Produce Lower Insertion Loss/Higher Isolation in Control Function Applications
SPDT3S PIN Diode Switch

Asymmetric Transmit/Receive (T/R) Design

Transmit Arm Optimized for Power Handling
- Single Series Diode for Reduced Insertion Loss
- Rectangular Anode for Improved Thermal Resistance

Receive Arm Optimized for Isolation
- Series/Shunt Configuration
- Shunt Diode Floating for Single Positive Supply Operation

GSG I/O Configuration for On-Wafer Characterization

**Test Vehicles**
DC Characterization

Rd (Slope Resistance)
- Pin4 to Pin5 – Tx PIN Diode
- Pin4 to Pin3 - Rx Series PIN Diode
- Pin3 to Pin2 – Rx Series/Shunt Combined PIN Diodes
- Pin1 to Pin2 – Rx Shunt PIN Diode

Results

SPDT3S – PIN Diode Switch

SPDT3S PIN Diode Switch

<table>
<thead>
<tr>
<th>V_{i1}</th>
<th>V_{i1}</th>
<th>Slope</th>
<th>V_{i2}</th>
<th>V_{i2}</th>
<th>Slope</th>
<th>V_{i3}</th>
<th>V_{i3}</th>
<th>Slope</th>
<th>V_{i4}</th>
<th>V_{i4}</th>
<th>Slope</th>
</tr>
</thead>
<tbody>
<tr>
<td>P4 to P5</td>
<td>P4 to P5</td>
<td>P4 to P5</td>
<td>P4 to P3</td>
<td>P4 to P3</td>
<td>P3 to P2</td>
<td>P3 to P2</td>
<td>P1 to P2</td>
<td>P1 to P2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>If=100mA</td>
<td>If=10mA</td>
<td>If=100mA</td>
<td>If=10mA</td>
<td>If=100mA</td>
<td>If=10mA</td>
<td>If=100mA</td>
<td>If=10mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SPDT3S Spec Limit</th>
<th>V_{i1}</th>
<th>V_{i1}</th>
<th>Slope Resistance</th>
<th>V_{i2}</th>
<th>V_{i2}</th>
<th>Slope Resistance</th>
<th>V_{i3}</th>
<th>V_{i3}</th>
<th>Slope Resistance</th>
<th>V_{i4}</th>
<th>V_{i4}</th>
<th>Slope Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.92V - 0.96V</td>
<td>0.65V - 0.90V</td>
<td>0.97V - 1.03V</td>
<td>0.65V - 0.90V</td>
<td>0.99V - 1.13V</td>
<td>0.65V - 0.90V</td>
<td>0.93V - 1.065V</td>
<td>0.65V - 0.90V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(mV)</td>
<td>(mV)</td>
<td>(mV)</td>
<td>(mV)</td>
<td>(mV)</td>
<td>(mV)</td>
<td>(mV)</td>
<td>(mV)</td>
<td>(mV)</td>
<td>(mV)</td>
<td>(mV)</td>
<td>(mV)</td>
<td>(mV)</td>
</tr>
</tbody>
</table>

<1-0-0> 0.0045 Ω-cm As Substrates
- 0.949 | 0.821 | 1.422 | 1.021 | 0.884 | 1.522 | 1.130 | 0.861 | 2.988 | 1.016 | 0.850 | 1.844 |

<1-1-1> 0.006 Ω-cm As Substrates
- 0.948 | 0.816 | 1.466 | 1.014 | 0.846 | 1.866 | 1.084 | 0.852 | 2.577 | 1.010 | 0.851 | 1.766 |

<1-1-1> 0.0017 Ω-cm P Substrates
- 0.955 | 0.817 | 1.533 | 1.050 | 0.851 | 2.211 | 1.241 | 0.870 | 4.122 | 1.048 | 0.851 | 2.188 |
Simplest Limiter Configuration

- Front End LNA Protection
- Single Stage Limiter – Limiting Turn-on a Function of PIN “I” Region Thickness
- Single Shunt PIN Diode with Return Coil
- Frequency Response – Diode Capacitance and Inductance of RF Return Coil
- Power Limiting is Approximately 10dB

Multi-Stage PIN Diode Limiters

- Higher Power Limiting
- Individual PIN Diodes for Optimal Characteristics
- Requires Multiple “I” Region Thicknesses
- Only Realized by Hybrid Assembly Techniques
- Power Limiting Approximately 10dB/Stage
HMIC Improvements
Multiple “I” Regions
Shunt PIN Diode

- Std HMIC Shunt PIN Diode

- Series/Shunt Switch Designs
  - Doped Mesa Sidewall, Metallic Sidewall Conductor, Frontside Cathode Contact Required

- Shunt Switches and PIN Limiter Designs
  - Doped Mesa Sidewall, Metallic Sidewall Conductor, Frontside Cathode Contact Optional

Standard HMIC Shunt Diode
**HMIC Improvements**

**Multiple “I” Regions**

**Lateral Diffusion Multiple “I” Region**

- Based on Std HMIC Shunt PIN Diode
- Series/Shunt, Shunt Switch & Limiter Designs
- Multiple “I” Regions Achieved by Sequential Anode Photo, Implantation, & Diffusion
- Capacitance Control by Anode Scaling/Lateral Diffusion Control
- Selective Optimization of Tx & Rx Switch Arms
- Monolithic Multi-Stage Limiters

Based on the Standard HMIC Shunt PIN Diode Structure
N+ Doped Sidewall, Metallic Sidewall Conductor, & Frontside Cathode Contact NOT Shown
Capacitance Control - Anode Scaling/Lateral Diffusion Control
HMIC Improvements
Multiple “I” Regions
HMIC Glass Multiple “I” Region

- Based on Std HMIC Shunt PIN Diode
- Shunt Switch & Limiter Designs
- Multiple “I” Regions Achieved by Sequential Anode Photo, Implantation, & Diffusion
- Surface Oxidation Required to Control Mesa Leakage
- Capacitance Control by HMIC Glass Isolation/Diameter Adjustment
- Selective Optimization of Tx & Rx Switch Arms
- Monolithic Multi-Stage Limiters

Based on the Standard HMIC Shunt PIN Diode Structure Requires Sidewall Oxidation to Control Surface/Vertical Leakage N+ Doped Sidewall, Metallic Sidewall Conductor, & Frontside Cathode Contact Not Allowed Capacitance Control - HMIC Glass to Adjust the Anode Diameters
HMIC PIN Diode Switches

- **Standard HMIC**
  - PIN Diode Configuration are Vertical Structures
  - Requires All PIN Diodes to Have a Common “I” Region Thickness (Epitaxially Grown)

- **Switch Arm RF Performance is a Compromise**

- **Typical HMIC SPDT Series/Shunt Schematic**

- **Series Element Prerequisite for Multi-Octave Bandwidth**

- **Monolithic SPST Through SP6T Configurations in HMIC**

- **IL/ISO/P\_1\_dB/Max Power Optimization Requires Variable “I” Region Thicknesses**
  - Thick “I”-Region => Power Handling/P\_1\_dB/High Iso
  - Thin “I”-Region => Low IL
HMIC Improvements
Multiple “I” Regions
Series PIN Diode

> Std HMIC Series PIN Diode

> Series/Shunt Switch Designs
  - Doped Mesa Sidewall, Metallic Sidewall Conductor, Frontside Cathode Contact Shunt Switches and PIN Limiter Designs
  - Doped Mesa Sidewall, Metallic Sidewall Conductor, Frontside Cathode Contact **Required**

> Backside Metallization
  - Full Area or Selectively Patterned
  - Primarily Mechanical Die Attach

---

**Standard HMIC Series Diode**
Multi “I” Region Thickness
HMIC Silicon Series PIN Diode

- Based on Std HMIC Series PIN Diode
- Series/Shunt & Series Switches
- Multiple “I” Regions Achieved by Sequential Anode Photo, Implantation, & Diffusion
- Capacitance Control by Anode Scaling/Lateral Diffusion Control
- Selective Optimization of Tx & Rx Switch Arms
Improvements to Basic HMIC Process Achieved Mixed Results

<1-0-0> and <1-1-1> Arsenic Substrates can be Employed Interchangeably

0.0017 Ω-cm Phosphorous Substrate - Schottky Diodes
- Reduced R<sub>d</sub> and R<sub>s</sub>
- Lower R<sub>s</sub> => Improved Mixer Conversion Loss
- Reduced RF loss => Improved Sensitivity

0.0017 Ω-cm Phosphorous Substrate - PIN Discrete Diodes
- Observed approximately 13% Reduction in High Frequency R<sub>s</sub>
- Reduced R<sub>s</sub> => Lower Insertion Loss/Higher Isolation in Control Function Applications

0.0017 Ω-cm Phosphorous Substrate - PIN Switches
- Expected Improvement in R<sub>s</sub> => Lower Insertion Loss/Higher Isolation
- RF Switch RF Characterization Required for Validation

Multiple Thickness “I” Region PIN Diodes
- Monolithic Multi-Stage Limiters – Higher Power Handling
- Optimize Tx Arm for Power Handling
- Improve Insertion Loss/Noise Figure in Rx Arm