Applications of 3D PEEC Solution to EMC Analysis and PCB Design Optimization

EMCoS LLC, Georgia
Contents:

- 3D PEEC Solver General Overview
- Advanced GUI and Smart Results Analysis
- Auto Merging of Electronic Circuit with 3D PEEC Equivalent Model of PCB Layout
- PCB Design Optimization Methodology and Workflow
- Impact of PCB Parasitic Parameters on Conducted Emission Test Results in Automotive LED Tail-light Application
- High Speed Connector Simulation
- Fast Simulation of PCB/IC/Flex Circuit Assembly
3D PEEC Solver General Overview

- To calculate mutual and self-inductances and resistances of branches, the 3D MoM-based Low Frequency Magnetic Field solver (LFMF) is used.
- To calculate mutual and self-capacitances of nodes, 3D MoM-based quasi-electrostatic solver (LFEF) is used.
- After all RLCG parameters are calculated, PEEC model is represented with lumped elements in SPICE format circuit file.
- The PEEC circuit can be combined with functional model. In practice, the functional circuit and PEEC model coupling procedure yields quite a complex circuit topology.
- The fast circuit simulation was fulfilled by developing a speed-oriented circuit solver, capable of simulating very large mixed networks consisting of millions of elements.

For electrically small systems quasi-static approximation can be used.
- Electrically small system size $\ll \lambda_{\text{max}}$
- Capacitance matrix is inverse of potential matrix: $C = \text{inverse}(P)$

Equivalent PEEC model of triangulated plate
(for simplicity of visualization mutual couplings between L and C elements are omitted from the picture)

- LOW
- MID
- HIGH

0+ Hz  10 kHz  10 MHz  100 MHz  1 GHz  5 GHz  10+ GHz
3D PEEC Solution Application Areas

PCB & IC Packages

Flex Cables & Connectors

HV Components (Batteries / Bus Bars /... )

EMC / EMI Filters
Advanced GUI and Smart Results Analysis for 3D PEEC Solution
Advanced GUI for 3D PEEC Solution

Merging of 3D PEEC Equivalent Circuit and Functional Scheme
Advanced GUI for 3D PEEC Solution

Fast Generation of PEEC Simulation Model for PCB Layout

1. Loading of PCB Layout
2. Automatic generation of pins and branches based on PCB footprints
3. Automatic partitioning of PCB nets based on pins location
4. Generation of PEEC equivalent circuit

- SAT
- IGES
- STEP
- CATIA V4&V5
- ODB++
- NASTRAN

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Advanced GUI for 3D PEEC Solution

Fast Generation of PEEC Simulation Model for PCB Layout

LOADING OF PCB LAYOUT

AUTOMATIC GENERATION OF PINS AND BRANCHES BASED ON PCB FOOTPRINTS

AUTOMATIC PARTITIONING OF PCB NETS BASED ON PINS LOCATION

GENERATION OF PEEC EQUIVALENT CIRCUIT

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Fast Generation of PEEC Simulation Model for PCB Layout

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4. Generation of PEEC Equivalent Circuit
Advanced GUI for 3D PEEC Solution

Fast Generation of PEEC Simulation Model for PCB Layout

The parasitic circuits extracted for all pins/branches are merged into a single equivalent circuit with corresponding number of output pins.
Visualization of equivalent circuits for each frequency point

RLC matrix viewer for deep analysis of calculation results

Hiding upper/lower triangular parts of the matrix

Matrices colormap visualization

Visualization of pin labels
Auto Merging of Electronic Circuit with 3D PEEC Equivalent Model of PCB Layout
New Features in 3D PEEC Solution

Auto Merging of Electronic Circuit with 3D PEEC Equivalent Model of PCB Layout

I scenario

II scenario

Import ODB++

PCB 3D Layout

Preprocessing

Cleaning and preprocessing of PCB layout

3D PEEC Model Generation

Automatic construction of 3D PEEC model from PCB layout and BOM data

3D PEEC Equivalent Circuit Extraction

Calculation of PCB layout equivalent circuit with 3D PEEC solver

Merging of Equivalent and Functional Schemes

Auto merging of 3D PEEC equivalent circuit and functional scheme of PCB

Complete Scheme

System level simulation of complete scheme

BOM Extraction

Cleaning and preprocessing of PCB layout

Automatic conversion of BOM data to Netlist device

Automatic conversion of BOM data to Netlist device

Functional Circuit Generation from BOM

Electronic circuit simulation with SPICE compatible solvers

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New Features in 3D PEEC Solution

BOM Extraction and Report Generation during ODB++ Import Procedure

Information about all PCB components and pins is translated from ODB++ to Excel spreadsheet – an essential part of automatic merging procedure
New Features in 3D PEEC Solution

Functional Circuit Extraction from BOM Table and Netlist Device Generation

Users have total control over circuit components directly from BOM table, with possibility to enable or disable specific components and pins. Components marked as “External” represent output pins of auto-generated netlist device, with possibility to attach S-parameters or SPICE models to them.
Automatic Construction of 3D PEEC Model from PCB Layout and BOM Data

PEEC model construction based on BOM data minimizes user intervention and automates the whole process.
Auto Merging of PCB Functional Scheme and 3D PEEC Equivalent Circuit

As the result of 3D PEEC calculation equivalent circuit of PCB layout will be automatically merged with functional scheme based on BOM data. Netlist device representing initial functional circuit can be easily substituted with complete scheme including all parasitic effects of PCB traces directly in System Diagram, preserving all the existing connections to other devices.
Application of 3D PEEC Solution to EMC Analysis and PCB Design Optimization
Impact of PCB Parasitic Parameters on Conducted Emission Test Results in Automotive LED Tail-light Application

REFERENCE:

“Impact of PCB Parasitic Parameters on Conducted Emission Test Results in Automotive LED Tail-light Application”,
A. Demurov¹,², G. Gabriadze¹,², I. Oganezova¹,², Z. Kutladze¹,², A. Gheonjian¹, F. Ajebar³, X. Bunlon³, I. Danelyan¹, R. Jobava¹,²
¹EMCoS LTD., Georgia; ²Tbilisi State University, Georgia; ³Renault S.A.S, France

The 19ème Colloque International et Exposition sur la Compatibilité ÉlectroMagnétique (CEM 2018)
Optimization Methodology and Workflow

Model Construction and 3D PEEC Simulation

System Simulation
- Merging of PCB equivalent circuit with functional scheme
- System simulation with complete design
- Analysis of the impact of PCB layout on filter performance

PCB Optimization Stage
- Improvements of PCB layout according to EMC design rules

Analysis Stage
- Identify critical regions from RLC matrices
- Current distribution analysis

END OF CYCLE
Impact of PCB Parasitic Parameters

Measurement Setup for Conducted Emission Test:

Conducted emission test was completed at EMCoS laboratory using test setup outlined in the CISPR 25 documentation.
Impact of PCB Parasitic Parameters

Simulation Model of Setup for Conducted Emission Test:

Configuration 1
Principal Circuit

System Diagram

LED lamp
connector
LISNs + battery

3D Viewer
Impact of PCB Parasitic Parameters

Measured and Simulated Results of Conducted Emission Test:

**Configuration 1**
Principal Circuit

![Circuit Diagram]

**Graph:**
- **X-axis:** Frequency (100kHz, 1MHz, 10MHz, 30MHz, 100MHz, 250MHz)
- **Y-axis:** Voltage [dBμV]
- **Measurements**
- **Simulations with principal circuit**

**Impact of PCB Parasitic Parameters**

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Impact of PCB Parasitic Parameters

Adjustment of Component Models:

Configuration 1
Detailed Components
Impact of PCB Parasitic Parameters

Measured and Simulated Results of Conducted Emission Test:

Configuration 1
Principal Circuit + Detailed Components

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Impact of PCB Parasitic Parameters

Generation of Equivalent Circuit for PCB Layout:

3D CAD Model of PCB

Configuration 1
PCB Layout

Output pins are generated based on PCB footprints (location of the components)
Impact of PCB Parasitic Parameters

Measured and Simulated Results of Conducted Emission Test:

Configuration 1
Principal Circuit + Detailed Components + PCB Layout

Simulations (Stage 2, PCB layout)
Simulations (Stage 1, Components)
Simulations (Principal circuit)
Measurements

Voltage [dB]

Frequency [Hz]
Charge and Field Distribution Analysis

Configuration 1: Charge Distribution (110 MHz)

Configuration 1: E Field Distribution (110 MHz)

Configuration 1: Charge Distribution (230 MHz)

Configuration 1: E Field Distribution (230 MHz)
Impact of PCB Parasitic Parameters

Modification of PCB Components:

Configuration 2
Additional Components
Impact of PCB Parasitic Parameters

Measured and Simulated Results of Conducted Emission Test:

Configuration 2
Principal Circuit + New Components + PCB Layout

![Configuration 2 Diagram]

![Voltage vs Frequency Graph]

- Measurements (Configuration 1)
- Simulations (Configuration 1)
- Measurements (Configuration 2)
- Simulations (Configuration 2)
Charge and Field Distribution Analysis

Configuration 1: Charge Distribution (110 MHz)

Configuration 2: Charge Distribution (110 MHz)

Configuration 1: E Field Distribution (110 MHz)

Configuration 2: E Field Distribution (110 MHz)
High Speed Connector Simulation with 3D PEEC Method

The project was done in collaboration with Missouri S&T EMC Laboratory.
High Speed Connector Simulation

High Speed Connector Overview

Measurements were done in Missouri S&T EMC Laboratory.
High Speed Connector Simulation

Simulation Model Overview for Full-Wave TriD Simulations

Simplified Simulation Model for Fullwave Analysis (4-port System)

- **Dielectric Part**
  - \( \varepsilon_r = 3.1; \tan(\delta) = 0.02 \)
  - \( \varepsilon_r = 4.19; \tan(\delta) = 0.025 \)

- **Metallic Part (PEC)**

**Legend**:
- Orange: Bulk dielectric
- Gray: Metallic objects
- Blue: Finite dielectric substrate

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High Speed Connector Simulation

Simulation Model Overview for Auto Partitioning 3D PEEC Simulations

Number of L elements = 915
Number of C elements = 609

Calculation Times

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<th>Calculation</th>
<th>Time</th>
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<td>L calculation (28,844 unkn.)</td>
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<tr>
<td>C Calculation (122,889 unkn.)</td>
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<td>Total (300 Freq. Samples)</td>
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</table>

- Total Number of Triangles = 91,949
- Number of Metallic Triangles = 59,637
- Number of Dielectric Triangles = 32,312
- 3mm is chosen for branch size
High Speed Connector Simulation

Simulation Results

Active Trace

Passive Trace
High Speed Connector Simulation

Simulation Results

Near End

Far End

Active Trace

Passive Trace
High Speed Connector Simulation

Simulation Results

Current Distribution at 1 GHz

Current Distribution at 4.5 GHz
Fast Simulation of PCB/IC/Flex Circuit Assembly with 3D PEEC Method

REFERENCE:

“Fast Simulation of PCB/IC/Flex Circuit Assembly Using Partial Element Equivalent Circuit Method”
G. Gabriadze\textsuperscript{1,2}, G. Chiqovani\textsuperscript{1}, A. Demurov\textsuperscript{1,2}, Z. Kutchadze\textsuperscript{1,2}, D. Karkashadze\textsuperscript{1,2}, R. Jobava\textsuperscript{1,2}
\textsuperscript{1}EMCoS LTD., Georgia; \textsuperscript{2}TIBILISI STATE UNIVERSITY, Georgia

The 2018 International Symposium on Electromagnetic Compatibility (EMC Europe 2018)
PCB/IC/Flex Assembly Simulation

Model Overview

- Controller and signal processing boards are connected using 180° rolled flex cable
- All metals are considered to be PEC
- Thickness of flex cable is 0.1 mm
- Flex strips width is 0.25 mm
- Distance between flex strips is 0.35 mm
- Relative dielectric permittivity of flex substrate is 2.7
- Both controlling and signal processing boards are printed on 1.57 mm thickness dielectric substrate, with relative dielectric permittivity 4.4
PCB/IC/Flex Assembly Simulation

Flex Cable Simulations

- Flex cable model contains 36,400 triangles. Average triangle size is 0.3 mm
- PEEC model with 3mm decomposition contains 149 inductance and 159 capacitance elements
PCB/IC/Flex Assembly Simulation

Simulation of Complete Assembly without Dielectrics

- PEEC model with 5 mm decomposition contains 366 inductance and 372 capacitance elements
- 50 Ohm ports are set on four pins of IC package and 50 Ohm loads at the end of corresponding circuit loops

Simulation model
(35,914 triangles, average triangle size 0.5mm)
PCB/IC/Flex Assembly Simulation

Simulation of Complete Assembly without Dielectrics (5 MHz)

Current Distribution

Charge Distribution

TriD

PEEC_3D

TriD

PEEC_3D
PCB/IC/Flex Assembly Simulation

Simulation of Complete Assembly without Dielectrics (5 MHz)
PCB/IC/Flex Assembly Simulation

Simulation of Complete Assembly with Dielectrics

- Simulation model with dielectrics contains 62,857 triangles. Average triangle size 0.5 mm
- PEEC model with 5mm decomposition contains 366 inductance and 372 capacitance elements

<table>
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<th>Memory [MB]</th>
<th>Time</th>
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<td>CG Calculation</td>
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Calculations are performed on a single 60 core Intel(R) Xeon(R) 2.5 GHz computer.
Thank you for your attention!